Designing of Switch-Limiter for X-Band Application in Discrete Components' Topology

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Abstract:

This paper presents a compact design technique of switch-limiter. PIN diodes are used as a basic design element. In blanking period, limiter path of Rx chain acts as a switch as it is intentionally biased. While in Rx mode it behaves as a normal limiter circuit. Few topologies are analyzed, like series, shunt-shunt, series-shunt etc with single and multiple numbers of diodes. Schematic level simulation is carried out in ADS. Approximate diode models are developed, also normalized susceptances are analyzed and plotted. A compact driver circuit is also designed using transistor-diode topology. It consists of two stages, where either a forward bias current or reverse bias voltage is being applied to PIN diodes.

Keywords: Limiter, Switch, Switch-Limiter, Blanking mode, Receiver protection, Spike leakage, Flat leakage.

[I] INTRODUCTION

RF and Microwave receivers are often at risk of having their front-ends burnt out by high power RF stray signals. Radar receivers require sensitive front-end circuits such as LNAs (Low Noise Amplifier) to process very weak signals with high gain to reduce the noise floor. Due to the sensitive nature, this circuit is often prone to damage if exposed to high level RF signals. Front-end protection circuits such as limiter and switch are often used to limit the level of intentional or unintentional RF signals [1]. Limiter and switch are generally placed in between the antenna and LNA. Most of them use the PIN diodes as power-controlled variable resistor.

The switch-limiter's function of protecting the receiver from high level signals while maintaining very low loss. This requires the use of a non-linear device. PIN diodes are commonly used because it can handle high power RF signals and provide reasonable leakage [2]. In the presence of small signals, the shunt diode does not conduct and therefore represents high impedance, or a low loss condition to the through path. In the presence of high power signals, the RF causes the diode to conduct; driving the impedance to drop well below the characteristic impedance of the device. Then the entire circuit becomes reflective. So majority of the input signal power reflects towards its source. The switch using PIN diodes have very short switching time (few tens of nanoseconds) and extremely compact in size. These diodes can switch at low power (few mili-watts), and high power level (up to kilo watts) at a much lower frequencies with low current levels (few mili-amps).

Switch-limiter behaves as a switch in Transmit (Tx) mode so there is no possibility of passing spike leakage towards LNA as it passes to 50Ω matched load. In Receive (Rx) mode it acts as a normal limiter. So in blanking mode antenna port mismatch really have no such impact in the receive path. Figure-1 shows a typical theoretical response of a limiter with high power fed at input.

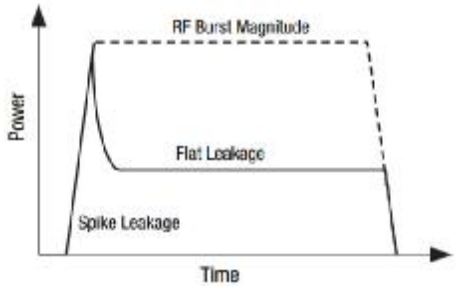

Figure-1 Response of a limiter with high power at input

Switching speed of a switch is a complex parameter which cannot be defined by only counting diodes' transition time. It depends on signal deliverability of the driver, meaning how fast the driver operates. So switching speed is a combination of driver and diodes' performance. This paper is categorized into five sections. First section covers Introduction. Second section deals extraction of diode modeling in brief. Section three describes the original switch-limiter and driver design techniques and implementation issues. Fourth Section

shows development of the switch-limiter & results. Last or Fifth section concludes about the switch.

[II] DIODE MODELING

Generally for diodes, manufacturers often do not support with exact models. Then designers have to find acceptable models [3,4] for its operating band-width.

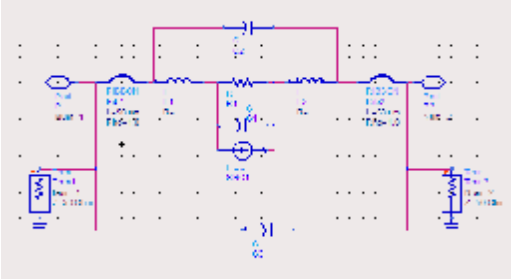

Figure-2 Approximated diode model in ADS

As models are not readily available, it is developed as per the data provided by manufacturers' datasheet. Figure-2 shows such a model. After extraction, these models have been used for microwave simulation.

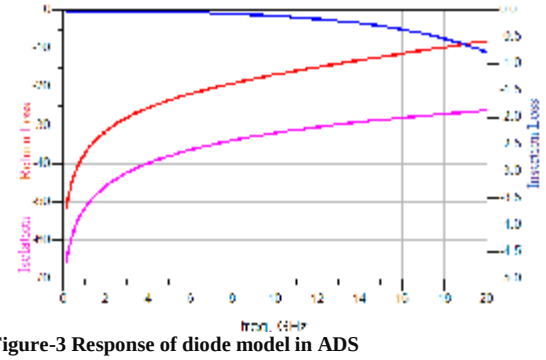

Figure-3 Response of diode model in ADS

Extraction of exact nonlinear model is difficult as few parameters are not mentioned in datasheet. Approximated models are made for the whole bandwidth [5]. For each diode, separate model is made, simulated and compared with its measured response. Necessary modifications are done in ADS model. Trend of these parameters are almost same as mentioned in the datasheets. Figure-3 shows response of a model simulated in ADS.

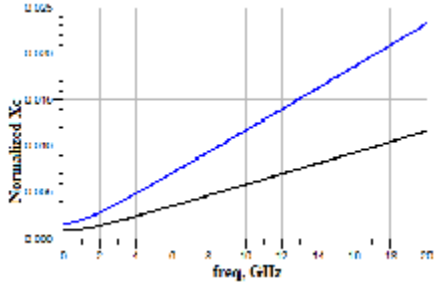

Figure-3 Normalized susceptance of diodes simulated in ADS

Normalized susceptance is analyzed for different diodes and plotted, as shown in Figure-4. Measured and analyzed susceptance values are compared to make better diodes' model.

[III] DESIGN APPROACH

Designing a switch-limiter for wide bandwidth with discrete components has different challenges. Proper diode and topology selection are one of the critical criteria. Insertion loss characteristic for shunt-shunt and series-shunt topology [3] is represented by equation (1) and (2) respectively in dB [¥¥].

$$I_{L_{sh}} = 10log\left[\left(1+\frac{R_{S1}}{2Z_0}\right)+\left(\pi f C_J\right)^2\left(Z_0+R_{S1}\right)^2\right]+\left(\frac{Z_0}{R_{p2}}\right) \quad (1)$$

$$I_{L_{se}} = 10log\left[\left(1+\frac{R_{S1}}{2Z_0}\right)+\left(\pi f C_J\right)^2\left(Z_0+R_{S1}\right)^2\right]+4\left(\frac{Z_0}{R_{p2}}\right) \quad (2)$$

As mentioned in above equations it is clear that loss in shunt-shunt topology is lesser that other one. In series mounted case as diode terminates in an open circuited, causing the line voltage to double across the diode and raising the insertion loss. Equation (3) and (4) describe about isolations in dB. It can be further processed by considering these conditions $R_{F2} \ll Z_0$ and $X_{L2} \ll Z_0$.

$$I_{iso_{se}} = 10log\left[\left(1+\frac{Z_0}{2R_{s1}}\right)^2+\frac{1}{4\pi f C_T Z_0}\left(1+\frac{Z_0}{R_{s1}}\right)^2\right] + 10log\left[\frac{\left(\frac{R_{F2}}{Z_0}+2\right)^2+\left(\frac{X_{L2}}{Z_0}\right)^2}{\left(\frac{R_{F2}}{Z_0}\right)^2+\left(\frac{X_{L2}}{Z_0}\right)^2}\right] \quad (3)$$

$$I_{iso_{sh}} = 10log\left[\left(1+\frac{Z_0}{2R_{s\,1}}\right)^2+\frac{1}{4\pi f C_T Z_0}\left(1+\frac{Z_0}{R_{s1}}\right)^2\right] + 10log\left[\frac{\left(\frac{1}{2}+\frac{R_{F2}}{Z_0}\right)^2+\left(\frac{X_{L2}}{Z_0}\right)^2}{\left(\frac{R_{F2}}{Z_0}\right)^2+\left(\frac{X_{L2}}{Z_0}\right)^2}\right] \quad (4)$$

Here diodes have been selected keeping in mind reverse breakdown voltage, power handling capability, switching speed, capacitance, forward resistance, carrier lifetime and thermal resistance. MP 6002 diode is selected for switch path and MA4L011 diode is for limiter purpose. Series resistance and capacitance values for these diodes are satisfactory over the operating bandwidth. Very low carrier lifetime is one more advantage for this design. Series-shunt and shunt-shunt topologies have been experimented. Finally shunt-shunt approach has been adopted as it provides better isolation and insertion loss for 8 to 11 GHz bandwidth [6,7,8]. Single and multiple numbers of diodes in each branch have also been experimented. As the number of element increases isolation meet better level for receiver protection, but insertion loss and size of the circuit becomes unrealizable for a specified area. Here insertion loss limits the use of maximum number of diodes. So isolation has also

linked with insertion loss. Trade-off is made in between insertion loss and isolation to fix the final design.

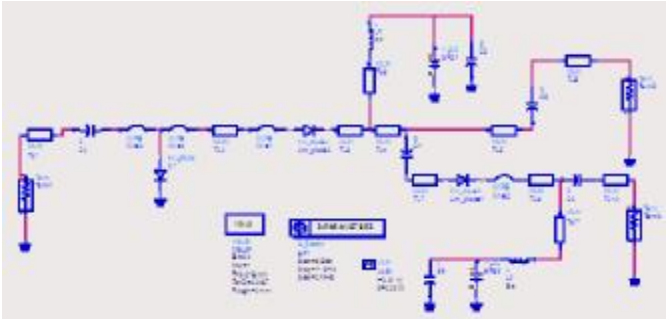

Figure-5a Series-shunt configuration of switch-limiter

Figure-5a and 5b show series- shunt and shunt-shunt topologies. These circuits are simulated in ADS. Gaps between tracks and lengths of the tracks are tuned very carefully keeping in mind broad band application in future.

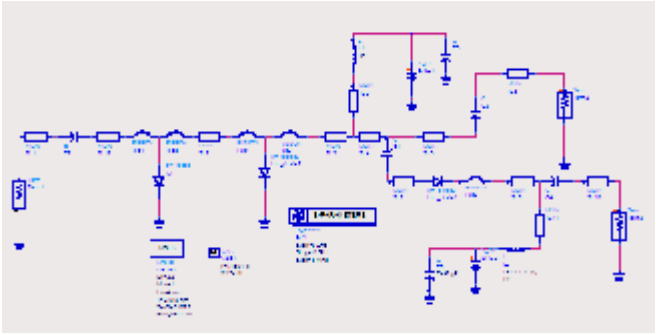

Figure-5b Shunt-shunt configuration of switch-limiter

It's interesting to compare the product of power handling and insertion loss for the shunt and series diodes respectively. In hard saturation power absorbed by series and shunt limiter diode is given in equation (5). Equation (6) and (7) indicate that the product of power handling and insertion loss is same whether diode is kept in series or shunt.

$$P_{D_{sh}} = P_L \frac{4R_{F2}}{Z_0} \quad and \quad P_{D_{se}} = P_L \frac{R_{F2}}{Z_0} \qquad (5)$$

so,

$$P_{D_{se}} X\, I_{L_{se}} = P_L \frac{R_{F_2}}{Z_0} X4 \left(\frac{Z_0}{R_{p2}}\right) = 4P_L \left(\frac{R_{F_2}}{R_{p2}}\right) \qquad (6)$$

$$P_{D_{sh}} X\, I_{L_{sh}} = P_L \frac{4R_{F_2}}{Z_0} X \left(\frac{Z_0}{R_{p2}}\right) = 4P_L \left(\frac{R_{F_2}}{R_{p2}}\right) \qquad (7)$$

In order to enhance power handling, it is possible to parallel n number of diodes to share the current. Thus, power handling varies directly with the power dissipation capability of the diode, line impedance, and the number of diodes used.

In figure-6 dotted and solid lines are indicating the data for series-shunt and shunt-shunt topologies

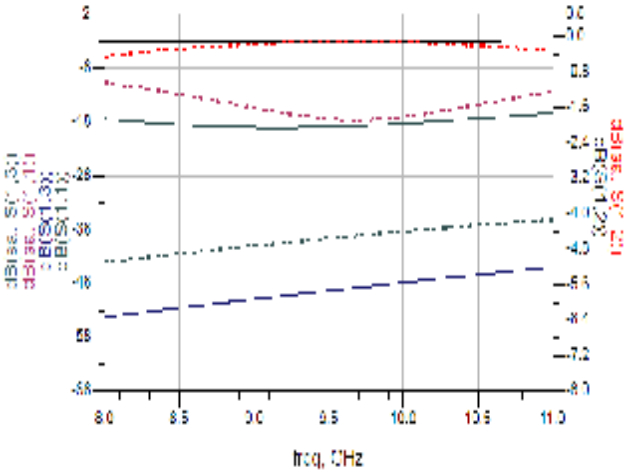

Figure-6 Comparative study between two topologies

respectively. Shunt-shunt configuration provides almost 10dB better isolation and more flat insertion loss characteristics over series-shunt topology for equal number of diodes. Non linear simulations are not possible as the models are not exactly non linear.

Present design requires very low insertion loss to improve receiver's noise figure. It is targeted to achieve noise figure less than 3.5 dB in the whole Rx chain. So noise figure for switch-limiter is expected to be less than 0.7 dB (excluding RF connector Loss). Maximum two diodes in shunt-shunt configuration secure sufficient isolation in blanking mode and insertion loss criteria of 0.7 dB.

As switching speed of the switch is a combination of driver and diodes performance. Proper driver circuit design is equally necessary to derive best switching performance [9]. Different techniques are available to design switch drivers. Simple transistor diode combination has been used to design the driver [5]. It consists two stages, where either a forward bias current or reverse bias voltage is to be applied to PIN diodes.

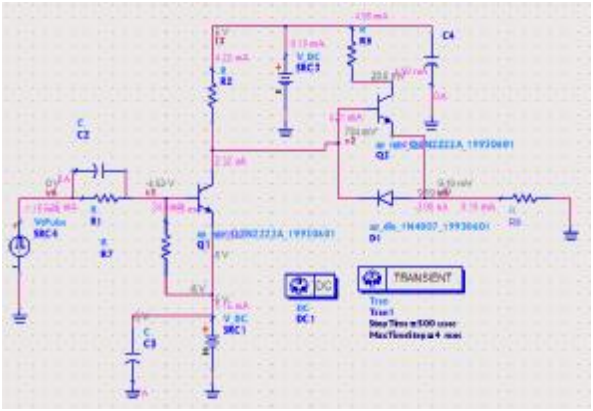

Figure-7 Schematics of Driver Circuit

The whole DC circuit is designed and simulated in LT Spice software. ADS simulation data is also satisfactory.

A suitable transistor has been selected keeping in mind the wide gain bandwidth product to deliver high speed bit streams without distortion. By pass elements and RF isolation chokes combination have been designed carefully to deliver undistorted pulse to PIN diodes. MMBT2222 transistor and 1N4148 diodes have been selected for design [5]. Figure-7 shows schematic design has done in ADS. LT spice design is equally satisfactory. DC annotation is also performed to check final voltage and current requirement. Figure-8 shows simulated result of driver.

As per DC annotation data, simulated response meets the requirement. Final schematics and layout for the switch-limiter is done in Eagle design software. Figure-7 does not show supply filtering scheme. Positive and negative supplies filtering have been taken care in the layout level.

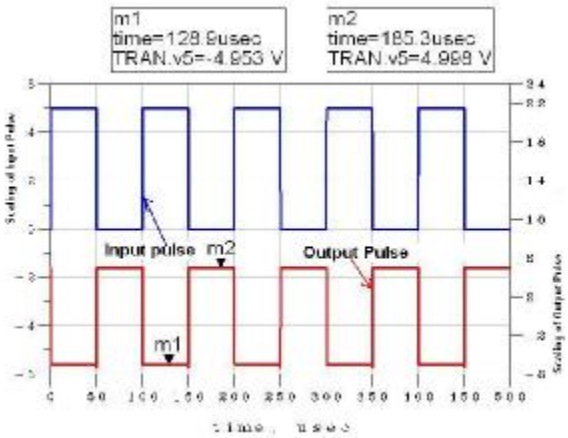

Figure-8 Simulated Response of Driver

It's a two layered board. This board and the switch-limiter are mounted on opposite sides of the housing. Control connections are taken from driver to switch side through small holes, keeping in mind the EMI/EMC effects.

Mechanical housing design is important for getting the expected response. Slot dimension of channel should be small enough to avoid higher mode excitation, which affects response at higher frequencies. Housing is made in compact size. Carrier plate has been made by keeping in mind smooth ground effects at higher frequencies as well as good mechanical strength to the PCB. It is made with 0.8 mm brass material.

[IV] EXPERIMENTATION

PCB of switch-limiters is realized on ½ oz Roger's material with a low dielectric constant, with enough gold plating. Driver circuit is fabricated on FR4 material. Wide range single layer capacitors are used to avoid unwanted troughs into the pass band. Isolation chokes are made with special care to avoid SRF for broad band applications.

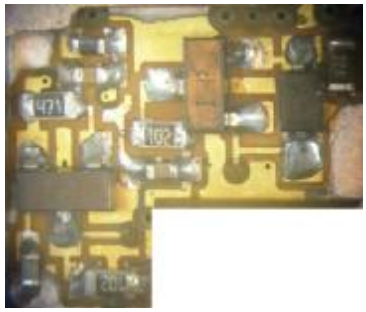

Figure-9 Developed Driver of Switch-limiter

Figure-9 shows the developed driver circuit. Measured response of driver of switch limiter shown in Fig-10. Response has glitches at the edges of the pulse which are due to long cables and that can be minimized by reducing wire length.

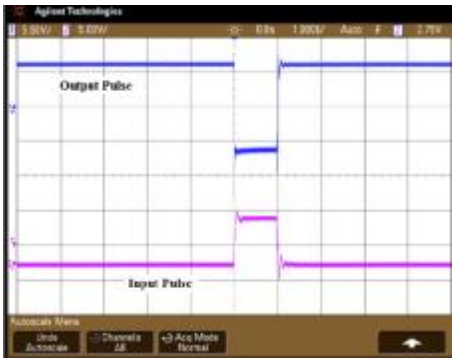

Figure-10 Measured Response of Driver

Switch-limiter is being tested final data will be attached in final presentation.

[V] CONCLUSION

Simulation and measured responses show that switch-limiter design with discrete components is possible if sufficient precautions and care are taken starting from simulation to final development. There will be difference between measurement and simulation response because of diode modeling in the simulation and actual diodes in the measurement. Practical diodes have tolerance values which were not considered in the simulation.

APPENDIX

¥ ¥ Diode parameters:

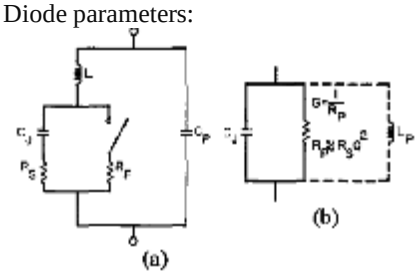

Figure-11 PIN diode equivalent circuit

$I_{L_{sh}}$	Insertion loss for shunt-shunt topology in dB
$I_{L_{se}}$	Insertion loss for series-shunt topology in dB
R_{s1}	Forward resistance of switch diode
f	Operating frequency
C_J	Junction capacitance
R_{p2}	Forward resistance of limiter diode placed in shunt configuration
Z_0	Line impedance of transmission line
R_{F2}	Reverse resistance when limiter is in hard saturation
X_{L2}	Reactive part of diode impedance; $Z=R_{F2}+X_{L2}$
$I_{iso_{se}}$	Isolation loss for series-shunt topology in dB
$I_{iso_{sh}}$	Isolation loss for shunt-shunt topology in dB
$P_{D_{sh}}$	Amount of absorbed power by diode in shunt mode
$P_{D_{se}}$	Amount of absorbed power by diode in series mode
P_L	Incident line power

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